DS04-13514-2E

Linear IC Converter

CMOS

D/A Converter for Digital Tuning

MB40D001

■ DESCRIPTION

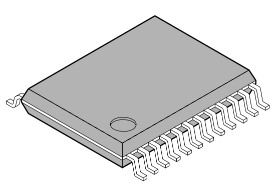
The MB40D001 is an 8-bit D/A converter with 12 built-in channels. The 12 sets of analog outputs have built-in OP amps to enable use with large current drive applications.
CS (chip select) data input/output format is used to enable connection to a serial bus. A built-in 12-bit I/O expander provides serial <=> parallel conversion (8 of the 12 bits are also used with analog output).
The MB40D001 can be adapted for microcontroller port expansion, or replacement of electronic volume control or semi-fixed calibration resistance.
Also, the MB40D001 is function- and pin-compatible with the MB88146A, for easy replacement when reducing sysytem operating voltage.

■ FEATURES

- Supply voltage 2.7 V to 3.6 V (Power consumption 0.7 mW/ch typ.)
- Compact package: SSOP-24
- R-2R type 8-bit D/A converter with 12 built-in channels
- Built-in 12-bit I/O expander (8 of 12 bits also used with analog output)
- Built-in analog amplifier (sink current max. 0.4 mA, source current max. 1.0 mA)
- Built-in power-on detector circuit (detects VccD power-on, and performs initialization)
- Separate MCU interface power supply (VccD), OP amp supply (VccA), D/A converter supply V_{DD}
- Analog output range 0 V to VccA.
- Serial data input/output operation to maximum of 2.5 MHz (1.5 MHz in cascade operation)
- CMOS process

■ PACKAGES

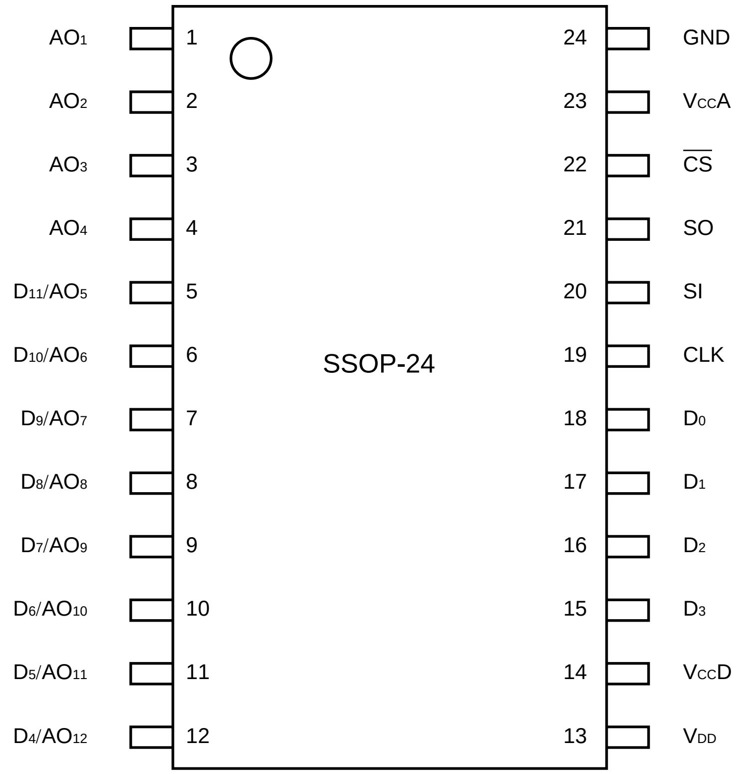
24-pin plastic SSOP



(FPT-24P-M03)

■ PIN ASSIGNMENT

(TOP VIEW)



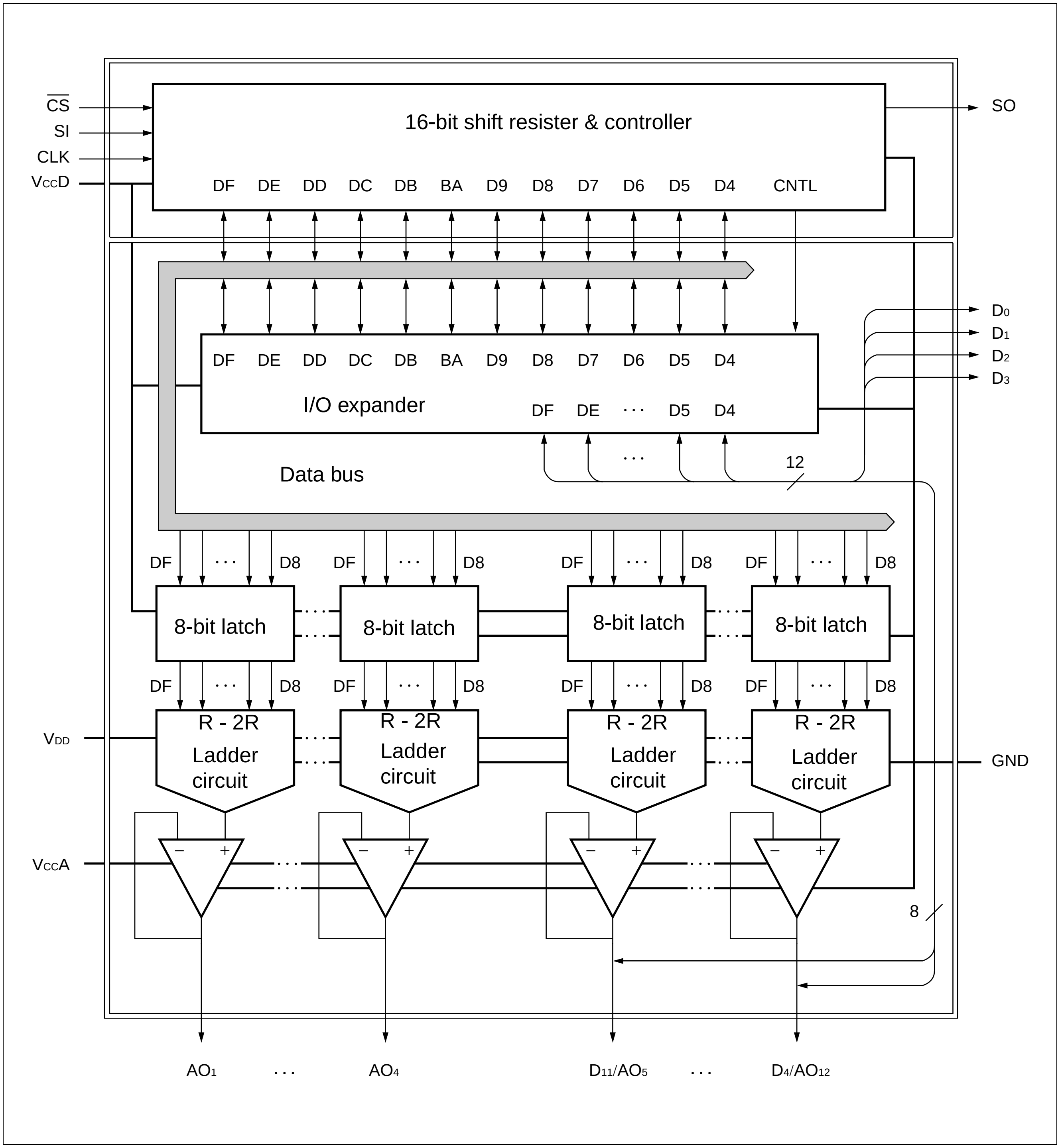
(FPT-24P-M03)

■ PIN DESCRIPTION

Pin no.	Symbol	Description
1 to 4	AO_1 to AO_4	D/A converter analog output pins (V_{DD}-GND output). (Default state: #00 setting level output)
5 to 12	D_{11}/AO_5 to D_4/AO_{12}	I/O expander parallel I/O pins (VccA/GND output 0.5 VccA/0.2 VccA input), also used as D/A converter analog output pins (V_{DD} - GND output). Pin state is controlled by input data. See "Data Configuration". (Default state: Input mode, high-impedance state.)
13	V_{DD}*1	D/A converter reference power supply pin.
14	$V_{CC}D$*1	MCU interface power supply (Power supply for I/O expander).
15 to 18	D_3 to D_0	I/O expander parallel I/O pins (VccD/GND output 0.5 VccD/0.2VccD input). Pin state is controlled by input data. See "Data Configuration". (Default state: Input mode, high-impedance state.)
19	CLK*2	Shift clock input pin. When $\overline{CS}$ = "L", SI data is loaded into the shift register at the rise of the shift clock signal.
20	SI*2	Data input pin (serial input pin). Used for 16-bit serial data input.
21	SO	Data output pin (serial output pin). First-bit (LSB) data from the 16-bit shift register is output in synchronization with the fall of the shift clock signal. When $\overline{CS}$ = "H", this pin is in high impedance state.
22	$\overline{CS}$*2	Chip select signal input pin. Input to shift registers is enabled when the $\overline{CS}$ signal falling edges. Shift register contents can be executed when the $\overline{CS}$ signal rising edges.
23	$V_{CC}A$*1	Analog unit power supply pin (Power supply for the OP amp.).
24	GND	Common GND pin.

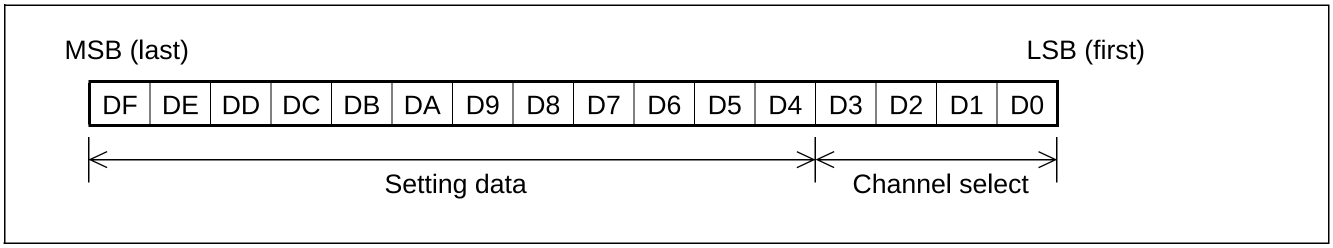
*1: Be sure that $V_{CC}A \geq V_{CC}D$, and that $V_{CC}A \geq V_{DD}$.
*2: Do not leave this pin in floating state.

■ BLOCK DIAGRAM



■ DATA CONFIGURATION

1. Data Configuration



2. Channel Select

D3	D2	D1	D0	Function
0	0	0	0	Don’t Care/special function
0	0	0	1	AO_1 selected
0	0	1	0	AO_2 selected
to	to	to	to	to
1	0	1	1	AO_{11} selected
1	1	0	0	AO_{12} selected
1	1	0	1	I/O expander (serial $\rightarrow$ parallel)
1	1	1	0	I/O expander (parallel $\rightarrow$ serial)
1	1	1	1	Expander status register (ESR)

3. Setting Data

• Don’t Care/special function (Channel select = “0000”)

DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Analog output voltage level
×	×	×	×	×	×	×	×	0	0	0	0	Don’t Care
to	to	to	to	to	to	to	to	to	to	to	to	Don’t Care
×	×	×	×	×	×	×	×	1	0	1	1	Don’t Care
0	0	0	0	0	0	0	0	1	1	0	0	GND (all channels)
0	0	0	0	0	0	0	1	1	1	0	0	$V_{DD}/256 \times 1$ (all channels)
0	0	0	0	0	0	1	0	1	1	0	0	$V_{DD}/256 \times 2$ (all channels)
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	1	0	1	1	0	0	$V_{DD}/256 \times 254$ (all channels)
1	1	1	1	1	1	1	1	1	1	0	0	$V_{DD}/256 \times 255$ (all channels)
×	×	×	×	×	×	×	×	1	1	0	1	High impedance (I/O expander state)*
×	×	×	×	×	×	×	×	1	1	1	0	Reset (state when power is ON)
×	×	×	×	×	×	×	×	1	1	1	1	Don’t Care

×: Don’t care   *: Hi-Z output on all channels of AO_5 through AO_{12}

• D/A Converter (Channel select = “0001” to “1100”)

DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Analog output voltage level
0	0	0	0	0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	0	0	0	0	$V_{DD}/256 \times 1$
0	0	0	0	0	0	1	0	0	0	0	0	$V_{DD}/256 \times 2$
0	0	0	0	0	0	1	1	0	0	0	0	$V_{DD}/256 \times 3$
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	0	1	0	0	0	0	$V_{DD}/256 \times 253$
1	1	1	1	1	1	1	0	0	0	0	0	$V_{DD}/256 \times 254$
1	1	1	1	1	1	1	1	0	0	0	0	$V_{DD}/256 \times 255$
×	×	×	×	×	×	×	×	0	0	0	1	High impedance (I/O expander state)*
×	×	×	×	×	×	×	×	0	0	1	0	Don’t Care
to	to	to	to	to	to	to	to	to	to	to	to	Don’t Care
×	×	×	×	×	×	×	×	1	1	1	1	Don’t Care

×: Don’t care   *: Only AO_5 through AO_{12} output is valid

- I/O Expander [Channel select = “1101”]: Serial → Parallel Conversion

  Performs parallel conversion of data bits D4 to DF for output on pins D_0 to D_{11}.
  Note that only those pins designated for output in the ESR (expander status register) are output.

Shift register

⇨	DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	⇨
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓					
	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Parallel I/O pins (output state)				

- I/O Expander [Channel select = “1110”]: Parallel → Serial Conversion

  Writes data from D_0 to D_{11} pins to bits D4 to DF in the shift register.
  Data is output to the SO pin on the shift clock (CLK) signal (The first 4 bits output data D0 to D3, so the converted output should be read as data bits 5 through 16.).
  Note that the data value is “0” for pins designated for output in the ESR (expander status register) as well as analog output pins.

Shift register

⇨	DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	⇨
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑					
	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Parallel I/O pins (output state)				

- Expander Status Register [Channel select = “1111”]

Shift register

⇨	DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	ESR
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	

This register sets the status of each pin.

Setting	Pin status
“0”	• Input standby status (Hi-Z output) • D_{11} to D_4 pins used for analog output should be set to “0”.
“1”	• Output state

Note: After power $V_{CC}D$ is turned ON (or after a reset), the state of pins and registers is as follows.

Pin	State
AO_1 to AO_4	"L" output
D_{11}/AO_5 to D_4/AO_{12}	Hi-Z state (input state)
D_3 to D_0	Hi-Z state (input state)

Register	State
Shift register	Bits DF to D8 are "0," and D7 to D0 are not defined (retain prior state).
D/A register	All reset to "0".
Parallel output register	Not defined (retain prior state).
Expander status register (ESR)	All reset to "0".

- ESR settings have priority in determining pin states. Switching between input standby state and analog output state is enabled even when the ESR value is "1". When the ESR value returns to "0", the pin returns to its previously defined state.
  In input standby state with AO set for Hi-Z output, the AO output setting can be used for transition to AO output state.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	$V_{CC}A$	Based on GND (Ta = +25°C)	–0.3	+7.0	V
	$V_{CC}D$		–0.3	+7.0	V
	V_{DD}		–0.3	$V_{CC}A$*	V
Input voltage 1	$V_{in}1$	SI, CLK, $\overline{CS}$, SO, D_0 to D_3	–0.3	$V_{CC}D$ + 0.3	V
Output voltage 1	$V_{out}1$		–0.3	$V_{CC}D$ + 0.3	V
Input voltage 2	$V_{in}2$	D_4 to D_{11}	–0.3	$V_{CC}A$ + 0.3	V
Output voltage 2	$V_{out}2$		–0.3	$V_{CC}A$ + 0.3	V
Power consumption	P_D	—	—	250	mW
Operating temperature	Ta	—	–20	+85	°C
Storage temperature	T_{stg}	—	–55	+150	°C

* : $V_{CC}A \geq V_{DD}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	$V_{CC}A$	—	2.7	3.0	3.6	V
	$V_{CC}D$	—	2.7	—	3.6	V
	V_{DD}	$V_{CC}A \geq V_{DD}$	2.0	—	$V_{CC}A$	V
	GND	—	—	0	—	V
Analog output current	I_{AL}	Source current	—	—	1.0	mA
	I_{AH}	Sink current	—	—	0.4	mA
Oscillation limit output capacity	C_{OL}	—	—	—	1.0	µF
Operation temperature	Ta	—	–20	—	+85	°C

Note: Data in registers is retained in standby mode (digital supply: VccD voltage, analog supply: GND).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTIC

1. DC Characteristics

(1) Digital section

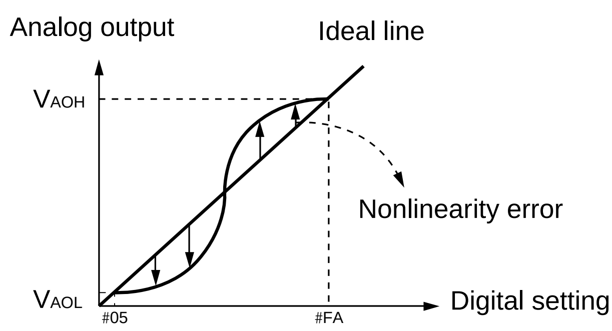
Parameter	Symbol	Pin name	Conditions	Value Min.	Value Typ.	Value Max.	Unit
Power supply voltage	$V_{CC}D$	$V_{CC}D$	—	2.7	3.0	3.6	V
Power supply current	$I_{CC}D$		CLK =1 MHz, (Unloaded)	—	0.1	0.35	mA
Standby current	$I_{CC}S$		CLK, SI, $\overline{CS}$ Stop V_{in} = $V_{CC}D$ or GND	–10	—	+10	µA
Input leak current	I_{ILK1}	CLK, SI, $\overline{CS}$, D_0 to D_3	V_{in} = 0 to $V_{CC}D$	–10	—	+10	µA
“H” level input voltage	V_{IH1}		—	0.5 × $V_{CC}D$	—	—	V
“L” level input voltage	V_{IL1}		—	—	—	0.2 × $V_{CC}D$	V
Output high-impedance leakage current	I_{OLK}	SO	V_{in} = 0 to $V_{CC}D$	–10	—	+10	µA
“H” level output voltage	V_{OH1}	SO, D_0 to D_3	I_{OH} = –0.4 mA	$V_{CC}D$ – 0.4	—	—	V
“L” level output voltage	V_{OL1}		I_{OL} = 2.5 mA	—	—	0.4	V

(2) D/A converter section

Parameter	Symbol	Pin name	Conditions	Value Min.	Value Typ.	Value Max.	Unit
Power supply voltage	V_{DD}	V_{DD}	$V_{DD} \leq V_{CC}A$	2.0	3.0	3.6	V
Power supply current	I_{DD}		$V_{DD} \leq V_{CC}A$	—	0.7	1.9	mA
Resolution	Res	AO_1 to AO_{12}	Unloaded	—	8	—	bit
Monotonic increase	Rem			—	8	—	bit
Nonlinearity error	LE			–1.5	—	+1.5	LSB
Differential linearity error	DLE			–1.0	—	+1.0	LSB

Nonlinearity error: Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at “05” and output voltage at “FA”.

Differential linearity error: Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note:The value of V_{AOH} and V_{DD}, and the value of V_{AOL} and GND are not necessarily equivalent.

(3) Operational Amplifier/Analog output section

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{CCA}	V_{CCA}	—	2.7	3.0	3.6	V
Power supply current	I_{CCA}		#80 setting (Unloaded)	—	1.0	4.8	mA
Input leakage current	I_{ILK2}	D_4 to D_{11}	V_{in} = 0 to V_{CC}A	–10	—	+10	µA
“H” level digital input voltage	V_{IH2}		—	0.5 × V_{CC}A	—	—	V
“L” level digital input voltage	V_{IL2}		—	—	—	0.2 × V_{CC}A	V
“H” level digital output voltage	V_{OH2}		I_{OH} = –0.4 mA	V_{CC}A – 0.4	—	—	V
“L” level digital output voltage	V_{OL2}		I_{OL} = 2.5 mA	—	—	0.4	V
Analog output minimum voltage 1	V_{AOL1}	AO_1 to AO_{12}	I_{AL} = 0 A #00 setting	GND	—	0.1	V
Analog output minimum voltage 2	V_{AOL2}		I_{AL} = 0.5 mA #00 setting	–0.2	GND	0.2	V
Analog output minimum voltage 3	V_{AOL3}		I_{AH} = 0.4 mA #00 setting	GND	—	0.15	V
Analog output minimum voltage 4	V_{AOL4}		I_{AL} = 1.0 mA #00 setting	–0.3	GND	0.3	V
Analog output maximum voltage 1	V_{AOH1}	AO_1 to AO_{12}	I_{AL} = 0 A #FF setting	V_{CC}A – 0.1	—	V_{CC}A	V
Analog output maximum voltage 2	V_{AOH2}		I_{AL} = 0.5 mA #FF setting	V_{CC}A – 0.2	—	V_{CC}A	V
Analog output maximum voltage 3	V_{AOH3}		I_{AH} = 0.4 mA #FF setting	V_{CC}A – 0.15	V_{CC}A	V_{CC}A + 0.15	V
Analog output maximum voltage 4	V_{AOH4}		I_{AL} = 1.0 mA #FF setting	V_{CC}A – 0.3	—	V_{CC}A	V

Note: I_{AH}: Analog output sink current I_{AL}: Analog output source current

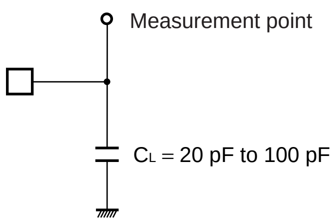
2. AC Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Clock “L” level pulse width	t_{CKL}	—	200	—	—	ns
Clock “H” level pulse width	t_{CKH}	—	200	—	—	ns
Clock rise time	t_{Cr}	—	—	—	200	ns
Clock fall time	t_{Cf}	—	—	—	200	ns
Serial input setup time	t_{SSU}	—	30	—	—	ns
Serial input hold time	t_{SHD}	—	60	—	—	ns
Serial output delay time	t_{SOD}	See “Load condition 1”*	0	120	300	ns
$\overline{CS}$ input setup time	t_{CSU}	—	100	—	—	ns
$\overline{CS}$ hold time	t_{CCH}	—	200	—	—	ns
$\overline{CS}$ “H” level hold time	t_{CSH}	—	100	—	—	ns
Data output enable time	t_{SO}	—	—	—	200	ns
Data output float time	t_{SOZ}	—	—	—	200	ns
Parallel input setup time	t_{PSU}	—	30	—	—	ns
Parallel input hold time	t_{PHD}	—	60	—	—	ns
Parallel output delay time	t_{POD}	See “Load condition 1”	—	120	300	ns
Analog output delay time	t_{AOD}	See “Load condition 2”	—	30	100	µs
Power supply rise time	t_R	—	—	—	50	ms
Power-on reset non-startup power supply variation	ΔV_R	—	–10	—	10	V/µs

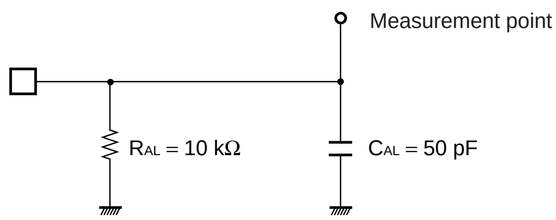
* : Cascade connection enabled at 1.5 MHz.

Load Conditions

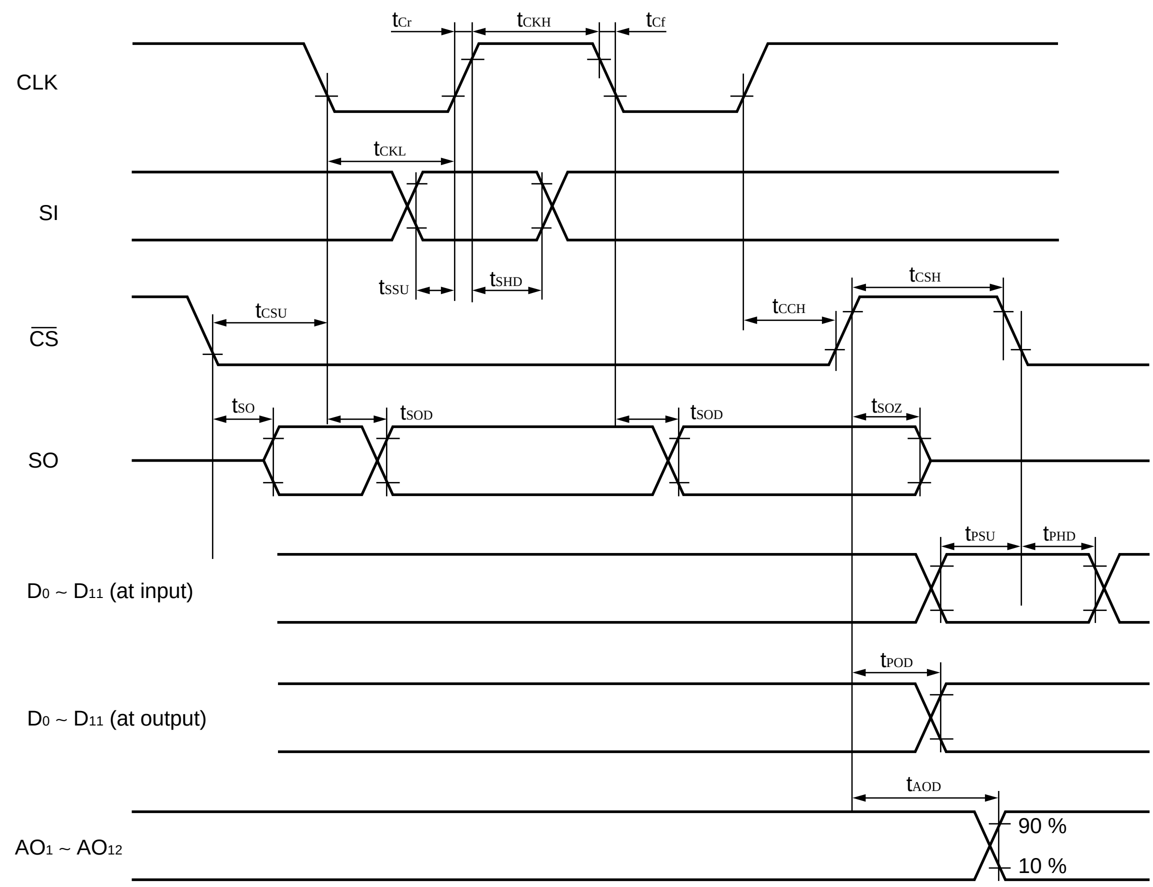
• Load condition 1



• Load condition 2



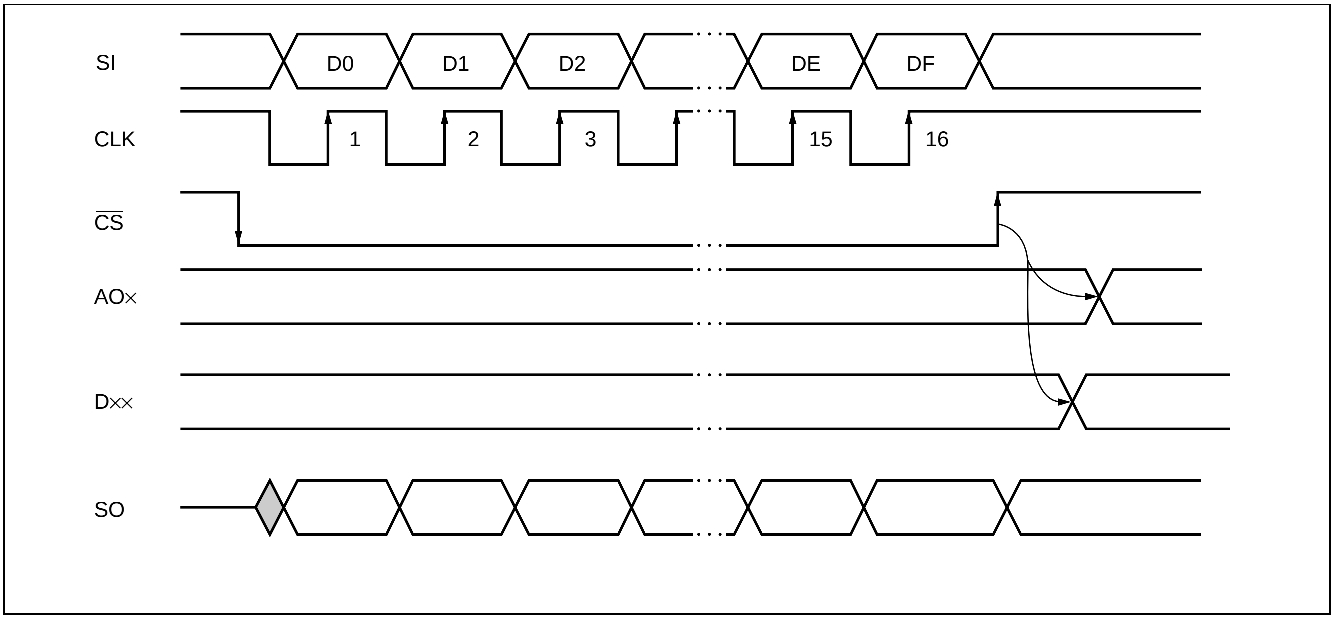
• Input/Output Timing ($\overline{CS}$ method)



CLK, SI, $\overline{CS}$, SO D_0 to D_3 decision level is 80% and 20% of VccD. D_4 to D_{11} decision level is 80% and 20% of VccA. AO_1 to AO_{12} decision level is 90% and 10% of VccA.

■ DATA INPUT/OUTPUT TIMING (Serial Bus Format)

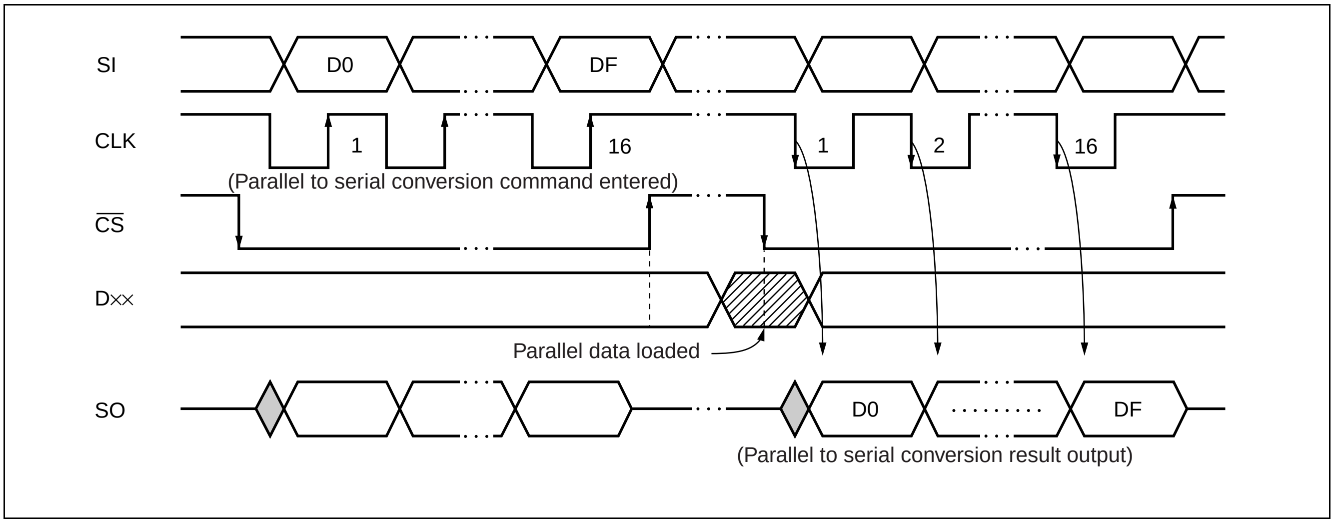
- Timing of D/A Converter Operation, I/O Expander Operation (serial to parallel conversion), and ESR Write Operation.



Data input is enabled at the fall of the $\overline{CS}$ signal. 16-bit data is input, and executed by shift register command at the rise of $\overline{CS}$.

In D/A converter operation, analog output selected at the rise of $\overline{CS}$ is converted. In serial to parallel conversion, digital output selected at the rise of $\overline{CS}$ is converted. In ESR write operation, data is set in the ESR at the rise of [CS] and used to change pin states.

- I/O Expander Operation (parallel to serial conversion)



Data input is enabled at the fall of the $\overline{CS}$ signal. 16-bit data (parallel to serial conversion command) is input, and commands received at the rise of $\overline{CS}$. At the fall of $\overline{CS}$ the data from parallel input is loaded in the shift register from D4 to DF, and output from the SO pin timed to the fall of the CLK signal.

■ USAGE PRECAUTIONS

1. Preventing Latch-Up

A condition known as “latch-up” may occur when the input or output pins of a CMOS IC device are exposed to voltages higher then $V_{CC}D$ or $V_{CC}A$ or lower than GND voltage, or when voltages are applied to the device in excess of rated values for $V_{CC}D$, VccA, or V_{DD} to GND voltages. Latchup produces a rapid increase in power supply current, and may result in thermal destruction of elements. Users should take sufficient precautions to ensure that absolute maximum ratings are not exceeded at any time during use.

2. Power Supply Pins

The power supply should be connected to the $V_{CC}D$, $V_{CC}A$, V_{DD}, and GND terminals of the IC with as low an impedance as possible.
In addition, it is recommended that ceramic capacitors of approximately 0.1 µF be connected as bypass capacitors between the $V_{CC}D$, $V_{CC}A$, and V_{DD} terminals and the GND terminals.

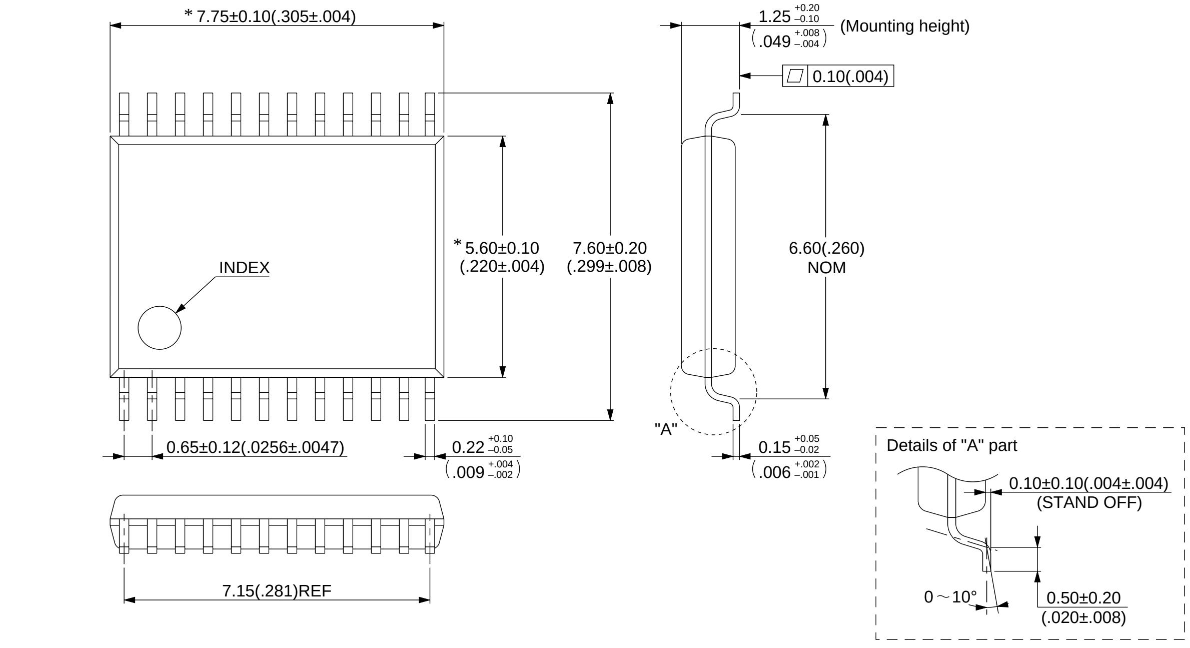
■ ORDERING INFORMATION

Part number	Package	Remarks
MB40D001PFV	24-pin Plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSIONS

24-pi plastic SSOP
(FPT-24P-M03)

*: These dimensions do not include resin protrusion.



Dimension in mm (inches)

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